REMARKS

The above-identified patent application has been amended and Applicant respectfully requests the Examiner to reconsider and again examine the claims as amended.

Claims 1-48 are pending in the application. Claims 35-44 are allowed. Claims 1-4, 7-16, 19-27, 30-34, and 45-48 are rejected. Claims 5, 6, 17, 18, 28, and 29 are objected to but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1, 12, 24, 35, and 45 are amended herein to correct a typographical error and not for reasons of patentability.

As an initial matter, Applicant notes that formal drawings earlier submitted on January 26, 2004 have been indicated in the Office Action as being approved by the Examiner. However, the Examiner's approval has not been indicated on the Office Action Summary PTOL-326 form. Approval of the drawings is respectfully requested.

The Rejections under 35 U.S.C. §102(b)

The Examiner rejects Claims 1-4, 7-16, 19-27, 30-34, and 45-48 under 35 U.S.C. §102(b) as being anticipated by Dwelley et al. (U.S. Patent number 6,166,527).

Applicant has amended independent Claims 1, 12, 24, and 45 (and also allowed claim 35) herein merely to correct an omission of a word "the" from each of the claims. The amendments are made merely to correct a typographical error, and not for reasons of patentability.

In the present application, as described, for example, in Claim 1, (also see, for example, FIG. 4) the claimed switching regulator comprises "...an inductor having first and second terminals, a first switch coupled between an input voltage and the first terminal of the inductor, a second switch coupled between the first terminal of the inductor and a first reference voltage, a third switch coupled between the second terminal of the inductor and the output node, and a

fourth switch coupled between the second terminal of the inductor and a second reference voltage." This arrangement is shown, for example, in FIG. 4.

Applicant submits that independent Claim 1 is patentably distinct over Dwelley et al., since the cited reference neither describes nor suggests "... a first state in which the first and third switches are closed and the second and fourth switches are open, a second state in which the second and third switches are closed and the first and fourth switches are open, and a third state in which the first and fourth switches are closed and the second and third switches are open; and *adjusting, in a first mode of operation, a number of state transitions from the first state to the second state relative to a number of state transitions from the first state to the third state* in response to the feedback signal," as set forth in Claim 1.

Referring to FIG. 9, states are described by the condition of four switches described above and denoted switches A-D. State AC corresponds to switches A and C being closed, which is representative of the claimed first state. State BC corresponds to switches B and C being closed, which is representative of the claimed second state. State AD corresponds to switches A and D being close, which is representative of the claimed third state.

Operation of the circuit of FIGS. 4 and 5 in the claimed first mode of operation, a buck-boost mode of operation (characterized by an input voltage close to a regulated output voltage), can be understood by referring to FIGS. 13-13B. In FIG. 13, it can be seen that the states transition in a sequence AC, BC, AC, AC, AD, AC, AC, BC, AC, AC, AD, AC, where the underlined portion corresponds to a repeating pattern of states when an error voltage, VCONT, is in a first voltage range. In FIG. 13A, it can be seen that the states transition in a sequence AC, BC, AC, AC, BC, AC, AC, AD, AC, AC, BC, AC, where the underlined portion corresponds to a repeating pattern of states when the error voltage, VCONT, is in a second voltage range. In FIG. 13B, it can be seen that the states transition in a sequence AC, AD, AC, AC, AD, AC, AC, BC, AC, AC, BC, AC, where the underlined portion corresponds to a repeating pattern of states when the error voltage, VCONT, is in a third voltage range. Therefore, in the first mode of operation, it will be understood that, to provide regulation, adjustment is made to the *number of*

state transitions from the first state to the second state relative to a number of state transitions from the first state to the third state.

In contrast, Dwelley et al. provides a switching regulator having four switches and having three states that follow a fixed state transition pattern in a buck-boost mode of operation, which can be identified in FIG. 6A to be AD, BD, AD, AC, AD, BD ..., where the underlined portion corresponds to a repeating pattern of states. Dwelley et al. does not adjust a number of state transitions as claimed. Instead, Dwelley et al. adjusts a duty cycle of the states to provide voltage regulation. Referring, for example, to FIG. 6A of Dwelley et al, switch control voltages V_A, V_B, V_C, V_D are shown in the above-described fixed repeating pattern. However, the duty cycle of certain ones of the states are changed (indicated by dashed lines) to provide the voltage regulation.

In view of the above, Applicant submits that Claim 1 is patentably distinct over Dwelley et al.

Claims 2-4 and 7-11 depend from and thus include the limitations of Claim 1. Thus, Applicant submits that Claims 2-4 and 7-11 are patentably distinct over the cited reference at least for the reasons discussed above in conjunction with Claim 1.

Applicant submits that Claim 2 is further patentably distinct over Dwelley et al., since the cited reference neither describes nor suggests "... said adjusting step comprises generating a digital waveform having a pulse rate proportional to the feedback signal," as set forth in Claim 2. Dwelley et al. describes no such proportional digital pulse rate.

Applicant submits that Claim 3 is further patentably distinct over Dwelley et al., since the cited reference neither describes nor suggests "... a sigma-delta converter," as set forth in Claim 3. A sigma-delta (or delta-sigma) converter 136 is shown in FIG. 5.

Applicant submits that Claim 7 is further patentably distinct over Dwelley et al., since the cited reference neither describes nor suggests "...a fourth state in which the second and fourth switches are closed and the first and third switches are open in response to an error condition," as set forth in Claim 7. The fourth state will be understood to correspond to a state BD. In contrast, as described above, Dwelley et al., for example in connection with FIG. 6A, describes only three states, and in connection with FIGS. 6B-6D described states for which only one of switches A and B is closed at a time. Dwelley et al. does not describe or suggest the claimed forth state, BD. The Examiner should be aware the Dwelley et al. labels his switches C and D in reverse of those of the present application. Therefore, the claimed fourth state requires switches B and C of Dwelley et al. to be closed, i.e., a state BC to Dwelley et al. Dwelley et al. does not describe or suggest this state.

Applicant submits that independent Claim 12 is patentably distinct over Dwelley et al., since the cited reference neither describes nor suggests "...generating first, second, third and fourth control signals to control the first, second, third, and fourth switches, respectively, in response to the feedback signal and to provide a first state in which the first and third switches are closed and the second and fourth switches are open, a second state in which the second and third switches are closed and the first and fourth switches are open, and a third state in which the first and fourth switches are closed and the second and third switches are open, wherein, *in a first mode of operation, a duty cycle of the first state within all periods of the periodic analog waveform corresponds to a first predetermined value, a duty cycle of the second state within periods of the periodic analog waveform in which the second state occurs corresponds to a second predetermined value, and a duty cycle of the third state within periods of the periodic analog waveform in which the third state occurs corresponds to a third predetermined value*," as set forth in Claim 12.

With this particular arrangement, again referring to FIGS. 13-13B, within any cycle of a periodic analog waveform, e.g., 544 (FIG. 13), the first state AC is seen to always have the same duration (e.g., the duty cycle approximately equals 75%), the second state, BC, when it occurs, is seen to always have the same duration (e.g., the duty cycle approximately equals 25%), and the

third state, AD, when it occurs, is seen to always have the same duration (e.g., the duty cycle approximately equals 25%).

In contrast, Dwelley et al, for example in FIG. 6A, shows states having variable duty cycles represented by dashed lines in the switch control voltages V_A, V_B, V_C, V_D. Dwelley et al. fails to describe or suggest the claimed duty cycles corresponding to predetermined values.

In view of the above, Applicant submits that Claim 12 is patentably distinct over Dwelley et al.

Claims 13-16 and 19-23 depend from and thus include the limitations of Claim 12. Thus, Applicant submits that Claims 13-16 and 19-23 are patentably distinct over the cited reference at least for the reasons discussed above in conjunction with Claim 12.

As described above in conjunction with Claim 2, Applicant submits that Claim 14 is further patentably distinct over Dwelley et al., since the cited reference neither describes nor suggests "... wherein said generating the first, second, third and fourth control signals comprises generating a digital waveform having a pulse rate proportional to the feedback signal," as set forth in Claim 14. As described above, Dwelley et al. describes no such proportional digital pulse rate.

As described above in conjunction with Claim 3, Applicant submits that Claim 15 is further patentably distinct over Dwelley et al., since the cited reference neither describes nor suggests "... a sigma-delta converter," as set forth in Claim 15. A sigma-delta (or delta-sigma) converter 136 is shown in FIG. 5.

As described above, in conjunction with Claim 7, Applicant submits that Claim 19 is further patentably distinct over Dwelley et al., since the cited reference neither describes nor suggests "...said generating the first, second, third and fourth control signals further provides a

fourth state in which the second and fourth switches are closed and the first and third switches are open in response to an error condition," as set forth in Claim 19.

Applicant submits that independent Claim 24 is patentably distinct over Dwelley et al., since the cited reference neither describes nor suggests "...generating first, second, third and fourth control signals to control the first, second, third, and fourth switches, respectively, in response to the feedback signal and to provide a first state in which the first and third switches are closed and the second and fourth switches are open, a second state in which the second and third switches are closed and the first and fourth switches are open, and a third state in which the first and fourth switches are closed and the second and third switches are open, wherein, *in a first mode of operation, state transitions consist of a transition from the first state to the second state and a transition from the second state to the first state in a first period of the periodic analog waveform and from the first state to the third state and from the third state to the first state in a second period of the periodic analog waveform*," as set forth in Claim 24.

This particular arrangement can be seen in FIG. 13, where within a cycle, e.g., cycle 544c, of the analog waveform 544, state transitions include transition AC, BC, AC, which corresponds to the first state to the second state to the first state. In another cycle, e.g., cycle 544b of the analog waveform 544, state transitions include transition AC, AD, AC, which corresponds to the first state to the third state to the first state.

In contrast, as shown, for example, in FIG. 6A of Dwelley et al., referring to the switch control voltages V_A, V_B, V_C, V_D, Dwelley et al. teaches three state transitions, the sequence of which is AD, BD, AD, AC, BD, AD..., where the underlined portion corresponds to a repeating pattern of states. It should be recognized that the C and D switches of Dwelley et al. are labeled in reverse to those of FIGS. 4 and 5 of the present invention. Even so, it can be seen that Dwelley et al. always provides three state transitions in sequence, regardless of the cycle of the analog waveforms V_X or V_Y. Dwelley et al. fails to describe or suggest the claimed state transition patterns.

In view of the above, Applicant submits that Claim 24 is patentably distinct over Dwelley et al.

Claims 25-27 and 30-34 depend from and thus include the limitations of Claim 24. Thus, Applicant submits that Claims 25-27 and 30-34 are patentably distinct over the cited reference at least for the reasons discussed above in conjunction with Claim 24.

As described above in conjunction with Claim 2, Applicant submits that Claim 25 is further patentably distinct over Dwelley et al., since the cited reference neither describes nor suggests "... said generating the first, second, third and fourth control signals comprises generating a digital waveform having a pulse rate proportional to the feedback signal," as set forth in Claim 25.

As described above in conjunction with Claim 3, Applicant submits that Claim 26 is further patentably distinct over Dwelley et al., since the cited reference neither describes nor suggests "...a sigma-delta converter," as set forth in Claim 26.

As described above, in conjunction with Claim 7, Applicant submits that Claim 30 is further patentably distinct over Dwelley et al., since the cited reference neither describes nor suggests "...generating the first, second, third and fourth control signals further provides a fourth state in which the second and fourth switches are closed and the first and third switches are open in response to an error condition," as set forth in Claim 30.

Applicant submits that independent Claim 45 is patentably distinct over Dwelley et al., since the cited reference neither describes nor suggests "...generating first, second, third and fourth control signals to control the first, second, third, and fourth switches, respectively, in response to the feedback signal and to provide a first state in which the first and third switches are closed and the second and fourth switches are open, a second state in which the second and third switches are closed and the first and fourth switches are open, and a third state in which the first and fourth switches are closed and the second and third switches are open, wherein, *during a*

single period of the periodic analog waveform, switches are in a selected two of the first, second, and third states," as set forth in Claim 45.

Again referring to FIG. 13, with the present arrangement, during a single period, e.g., period 544c of the analog waveform 544, only two states are provided. For the period 544c, the states are AC and BC. Similarly, other periods of the analog waveform 544 are also associated with but two states.

In contrast, in Dwelley et al., for example in FIG. 6A, the switch control voltages V_A, V_B, V_C, V_D have *three* states within a period of the analog waveforms V_X or V_Y, not the claimed two states.

In view of the above, Applicant submits that Claim 45 is patentably distinct over Dwelley et al.

Claims 46-48 depend from and thus include the limitations of Claim 45. Thus, Applicant submits that Claims 46-48 are patentably distinct over the cited reference at least for the reasons discussed above in conjunction with Claim 45.

For substantially the same reasons discussed above in conjunction with Claim 1, Applicant submits that Claim 46 is further patentably distinct over Dwelley et al., since the cited reference neither describes nor suggests "... a number of state transitions from the first state to the second state are adjusted relative to a number of state transitions from the first state to the third state in response to the feedback signal," as set forth in Claim 46.

For substantially the same reasons discussed above in conjunction with Claim 12, Applicant submits that Claim 47 is further patentably distinct over Dwelley et al., since the cited reference neither describes nor suggests "...a duty cycle of the first state within all periods of the periodic analog waveform corresponds to a first predetermined value, a duty cycle of the second state within periods of the periodic analog waveform in which the second state occurs

corresponds to a second predetermined value, and a duty cycle of the third state within periods of the periodic analog waveform in which the third state occurs corresponds to a third predetermined value," as set forth in Claim 47.

For substantially the same reasons discussed above in conjunction with Claim 24, Applicant submits that Claim 48 is further patentably distinct over Dwelley et al., since the cited reference neither describes nor suggests "... state transitions consist of a transition from the first state to the second state and a transition from the second state to the first state in a first period of the periodic analog waveform and from the first state to the third state and from the third state to the first state in a second period of the periodic analog waveform," as set forth in Claim 48.

In view of the above, Applicant submits that the rejection of Claims 1-4, 7-16, 19-27, 30-34, and 45-48 under 35 U.S.C. §102(b) should be removed.

The Claim Objections

The Examiner objects to Claims 5, 6, 17, 18, 28, and 29 as being dependent upon a rejected base claim, but indicates that Claims 5, 6, 17, 18, 28, and 29 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

For the above reasons, Applicant submits that independent Claim 1, from which Claims 5 and 6 depend, independent Claim 12, from with Claims 17 and 18 depend, and independent Claim 24, from which Claims 28 and 29 depend, are patentably distinct over the cited references. Therefore, Applicant submits that Claims 5, 6, 17, 18, 28, and 29 are allowable in their present dependent form.

In view of the above Amendment and Remarks, Applicant submits that the claims and the entire case are in condition for allowance and should be sent to issue and such action is respectfully requested.

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Reply to Office Action of November 29, 2004

Docket No. ALLEG-042PUS

The Examiner is respectfully invited to telephone the undersigning attorney if there are any questions regarding this Amendment or this application.

The Assistant Commissioner is hereby authorized to charge payment of any additional fees associated with this communication or credit any overpayment to Deposit Account No. 500845, including but not limited to, any charges for extensions of time under 37 C.F.R. §1.136.

Respectfully submitted,

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